Amendments to the Drawings:

Figure 4 is added to show the features of a third storage block. Figure 4 now shows first, second, and third storage blocks 58, 59, 60. Paragraph [0014.1] is added to reflect this change, and paragraphs [0029] to [0031] have also been amended accordingly.

Acceptance of the drawings and the amended specification is respectfully requested.

Attachment: New Sheet 1 page

REMARKS/ARGUMENTS

1. Claims 5, 7, 15, 19, and 27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Response:

Regarding the rejection of claim 5, the limitations previously found in claim 5 have been added to claim 1. Claim 1 now recites "the bus interface circuit preventing the controller from transferring data to the bus interface" to clarify what is preventing the controller from transferring data. In view of this clarification, claim 1 should be free of any indefinite language.

Regarding the rejection of claims 7, 15, and 27, the registered trademark PCIX has been deleted from claims 7 and 15, and claim 27 has been cancelled.

Regarding the rejection of claim 19, claim 19 has also been cancelled, and is no longer in need of consideration.

2. Claims 1-4, 6, 8-14, 16-22, and 24-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Kanda (US 2002/0138697).

Response:

Claims 19-29 have been cancelled, and are no longer in need of consideration. Independent claims 1 and 11 have been amended to overcome the claim rejections.

Each of claims 1 and 11 now specifies that the bus interface circuit contains a third storage block, and that "before data stored in the first storage block are completely

outputted to the bus, the bus interface circuit prevents the controller from transferring data to the bus interface circuit if the second and third storage blocks are full". None of the cited prior art teaches these limitations. In addition, the examiner indicated that claim 5 would be allowable if rewritten to overcome the rejection under 35 U.S.C. 112, second paragraph and to include all of the limitations of the base claim and any intervening claims.

In view of the amendments to independent claims 1 and 11, the applicant submits that all claims are now in allowable form. Dependent claims 6-10, 12, and 14-18 are dependent on claims 1 and 11, and should be allowed if claims 1 and 11 are allowed. Reconsideration of claims 1, 6-12, and 14-18 is respectfully requested.

3. Introduction to new claims 30-32:

New claims 30 and 31 each state that a transfer rate between the controller and the bus interface circuit is not less than the data transfer rate between the bus interface circuit and the bus. This limitation is fully supported in paragraphs [0010] and [0032] of the instant application, and no new matter is added.

On the other hand, Kanda teaches in paragraph [0062], "As already explained, the HDD I/F A 202a to HDD I/F D 202d each comprises a pair of toggle FIFO memories 403 in the respective one of the DMA data control sections 402a to 402d such that differences in transfer rates between the HDD A 107a to HDD D 107d can be compensated."

Thus, Kanda discloses that each HDD interface has two FIFO memories to compensate the differences in transfer rate between the HDDs. On the other hand, the instant application discloses using a plurality of buffers to store data waiting to be transferred, and the data transfer rate between the controller and the bus interface is not less than the data transfer rate between the bus interface and the bus. Therefore, the

device can continuously occupy the external bus without entering a waiting state (paragraph [0010]).

In paragraph [0065], Kanda discloses that if one memory is full and the other one is transferring data to HDD, the data from the CPU-DMA I/F section is no longer transferring data to the memory. However, Kanda doesn't disclose that the data transfer rate between the CPU-DMA I/F and the HDD I/F is not less than the data transfer rate between the HDD I/F and the HDD. Thus, new claims 30-32 should be allowable over Kanda. Acceptance of new claims 30-32 is respectfully requested.

The applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

/Winston Hsu/ Date: 05/30/2006

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